AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs:

[0027] Image sensors implementing pixel cells having increased storage, with decreased size are disclosed in co-pending U.S. application Nos. 10/721,190 ~~[M4065.0852]~~ and 10/721,191 ~~[M4065.0902]~~ which are incorporated herein by reference. U.S. application No. 10/721,190 ~~[M4065.0852]~~ relates to an image sensor implementing pixel cells having an electronic shutter which includes a shutter transistor having its gate electrically connected to a storage capacitor. U.S. application No. 10/721,191 ~~[M4065.0902]~~ relates to an image sensor implementing pixel cells having an electronic shutter which includes a gated storage node.

[0042] Pixel cells 200 and 400 can be implemented in an imager and operated as described in incorporated co-pending U.S. application Nos. 10/721,190 ~~[M4065.0852]~~ and 10/721,191 ~~[M4065.0902]~~, with the added advantage that pixel cells according to embodiments of the present invention each include an anti-blooming transistor 211, 411.

[0045] By connecting transfer gates 616, 716 to anti-blooming gates 611, 711, pixel cells 600 and 700 may have fewer signal lines than are required for pixel cells 200 and 400, respectively. For purposes of this specification, the term "signal lines" refers to lines, for example metal lines, that ~~?hat~~ carry signals to or from devices of a pixel cell. Additionally, tying the drain of the anti-blooming gates 611 and 711 to V_{aa_pix} also serves to improve the size of pixel cells 600 and 700 by keeping the number of signal lines to a minimum. Pixel cells 600 and 700 are each able to employ an anti-blooming transistor without adding additional signal lines to the pixel cells disclosed in the aforementioned U.S. application Nos. 10/721,190 ~~[M4065.0852]~~ and 10/721,191 ~~[M4065.0902]~~.

[0059] FIGS. 9A-10B are schematic diagrams of multiplexed pixel cells according to exemplary embodiments of the invention and depict two or more pixel cells sharing a floating diffusion node and readout and reset circuitry. U.S. application Nos. 10/721,190 ~~[M4065.0852]~~ and

10/721,191 ~~[M4065.0902]~~, incorporated herein, disclose two or more pixel cells sharing a sensing node, e.g., a floating diffusion node, and pixel readout and reset circuitry. For purposes of this specification, the term "pixel readout and reset circuitry" refers to any circuitry within a pixel cell which serves to readout photo-generated charge from a sensing node, or to reset the sensing node to a predetermined voltage. FIGS. 9A through 10B, however, also show an anti-blooming transistor in each pixel cell.